CLAIMS AS AMENDED

1. (amended) A procedure for the manufacture of a bi-polar transistor, during which structured regions consisting of a collector region and an insulation region that surrounds the collector region are produced on a monocrystal substrate layer, a base layer and, by means of epitaxy, a cap layer are produced over the collector region where an interposed buffer layer can be deposited, an insulation layer is deposited over the cap layer, the insulation layer is opened in the area of the effective emitter zone, a poly-Si or an α-Si layer is deposited and structured over the opened insulation layer and is then used as an emitter-doping agent source and as a contact layer, wherein, before the diffusion from the emitter-doping agent source, a doping profile is introduced into the cap layer, and the profile is low-doped on the base side and highly doped on the emitter side.

2. (amended) The procedure according to claim 1, wherein the base-side lower doping concentration of the cap layer does not exceed values of 5×10^{16} cm^{-3}.

3. (amended) The procedure of claim 1, wherein the cap layer is of a thickness between 20 nm and 70 nm.

4. (amended) The procedure of claim 1, wherein the emitter-side high doping concentration of the cap layer does not exceed values of 5×10^{18} cm^{-3} when the doping agent is of the same conductivity type as the base layer.

5. (amended) The procedure of claim 1, wherein the cap doping profile is introduced by implantation.

6. (amended) The procedure of claim 1, wherein the cap doping profile is introduced in situ during the epitaxy process.

7. (amended) The procedure of claim 1, wherein the cap doping profile is introduced by diffusion from the insulation layer after highly enriching the insulation layer with the doping agent.

8. (amended) A bi-polar transistor, in which structured regions consisting of a collector region and an insulation region that surrounds the collector region are produced on a monocrystal substrate layer, a base layer and , where a buffer layer can be interposed, by means of epitaxy, a cap layer are produced over the collector zone, an insulation layer is deposited over the cap layer, the insulation layer is opened in the area of the effective emitter zone, a poly-Si or an α-Si layer is deposited and structured over the opened insulation layer and is then used as an emitter-doping agent source and as a contact layer,

wherein, in an overlapping region between an edge of the emitter window and the outer delimitation of the structured poly-silicon or α-silicon layer the cap layer contains a doping profile, and the profile is low-doped on the base side and highly doped on the emitter side.

9. (amended) The bi-polar transistor according to claim 8, wherein the base-side lower doping concentration of the cap layer does not exceed values of 5×10^{16} cm^{-3}.

10. (amended) The bi-polar transistor of Claim 8, wherein the cap layer is of a thickness between 20 nm and 70 nm.

11. (amended) The bi-polar transistor of Claim 8, wherein the emitter-side high doping concentration of the cap layer does not exceed values of 5×10^{18} cm^{-3} when the doping agent is of the same conductivity type as the base layer.

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12. (new) A procedure for manufacturing a bi-polar transistor, comprising the steps of:

producing, on a monocrystal substrate layer, structured regions consisting of a collector region and an insulation region, the insulation region surrounding the collector region,

producing a base layer and a cap layer over the collector region, the cap layer produced by epitaxy;

depositing an insulation layer over the cap layer, the insulation layer opened in an area of an effective emitter zone; and

depositing and structuring a poly-Si or an α-Si layer over the opened insulation layer, and using this layer as a source of emitter-doping agent and as a contact layer;

wherein, before diffusing from the emitting-doping agent source, a doping profile is introduced into the cap layer, the profile being low doped on a base side thereof and high doped on an emitter side thereof.

13. (new) The procedure of claim 12, further comprising the step of depositing a buffer layer between the collector region and the base layer.

14. (new) A bi-polar transistor, comprising:

a monocrystal substrate layer;

structured regions comprising a collector region and an insulation region surrounding the collector region atop the monocrystal substrate layer;

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a base layer and, by means of epitaxy, a cap layer produced over the collector region when a buffer layer can be interposed;

an insulation layer deposited over the cap layer, the insulation layer being opened in an area of an effective emitter zone; and

a poly-Si or an α-Si layer deposited and structured over the opened insulation layer, this layer then used as an emitter-doping agent source and as a contact layer,

wherein, in an overlapping region between an edge of the emitter zone and an outer delimitation of the structured poly-silicon or α-silicon layer, the cap layer contains a doping profile, and the profile is low-doped on a base side thereof and highly doped on an emitter side thereof.